EAST SEARCH

4/14/04

L#	Hits	Search String	Databases
L1	14211	power and distribution and (cell or index or matrix) and node	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	387	1 and (703/$.ccor. or 716/$.ccor.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	58	2 and (power adj distribution)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	33	5404310.uref.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	16	5537328.uref.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L6	64	('i/o' adj cell) same placement	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

Results of search set L3:

US 6662149 B1	Method and apparatus for efficient computation of moments in interconnect circuits	20031209	703/14
US 6584596 B2	Method of designing a voltage partitioned solder-bump package	20030624	716/1
US 6577992 B1	Transistor level circuit simulator using hierarchical data	20030610	703/14
US 6564355 B1	System and method for analyzing simultaneous switching noise	20030513	716/4
US 6557154 B1	Printed circuit board design support system, printed circuit board design method and storage medium storing control program for same	20030429	716/11
US 6532439 B2	Method for determining the desired decoupling components for power distribution systems	20030311	703/14
US 6530065 B1	Client-server simulator, such as an electrical circuit simulator provided by a web server over the internet	20030304	716/4
US 6523154 B2	Method for supply voltage drop analysis during placement phase of chip design	20030218	716/6
US 6523150 B1	Method of designing a voltage partitioned wirebond package	20030218	716/4
US 6510545 B1	Automated shielding algorithm for dynamic circuits	20030121	716/12
US 6480986 B1	IC substrate noise modeling including extracted capacitance for improved accuracy	20021112	716/4
US 6467074 B1	Integrated circuit architecture with standard blocks	20021015	716/17
US 6453444 B1	Method for extraction of inductances in integrated circuits	20020917	716/2
US 6438733 B1	IC substrate noise modeling with improved surface gridding technique	20020820	716/4
US 6438729 B1	Connectivity-based approach for extracting layout parasitics	20020820	716/1
US 6421814 B1	Method of extracting layout parasitics for nets of an integrated circuit using a connectivity-based approach	20020716	716/5

US 6385565 B1	System and method for determining the desired decoupling components for power distribution systems using a computer system	20020507	703/18
US 6308304 B1	Method and apparatus for realizable interconnect reduction for on-chip RC circuits	20011023	716/5
US 6253165 B1	System and method for modeling probability distribution functions of transform coefficients of encoded signal	20010626	703/2
US 6249898 B1	Method and system for reliability analysis of CMOS VLSI circuits based on stage partitioning and node activities	20010619	716/4
US 6209122 B1	Minimization of circuit delay and power through transistor sizing	20010327	716/6
US 6128768 A	Method of extracting layout parasitics for nets of an integrated circuit using a connectivity-based approach	20001003	716/5
US 6072945 A	System for automated electromigration verification	20000606	716/5
US 5999726 A	Connectivity-based approach for extracting layout parasitics	19991207	716/11
US 5963729 A	Method for automated electromigration verification	19991005	716/5
US 5949988 A	Prediction system for RF power distribution	19990907	703/2
US 5903469 A	Method of extracting layout parasitics for nets of an integrated circuit using a connectivity-based approach	19990511	716/5
US 5880968 A	Method and apparatus for reducing power usage within a domino logic unit	19990309	716/5
US 5872952 A	Integrated circuit power net analysis through simulation	19990216	703/14
US 5828580 A	Connectivity-based approach for extracting parasitic layout in an integrated circuit	19981027	716/12
US 5781764 A	Method and apparatus for generation a system component model and for evaluation system parameters in relation to such model	19980714	703/2
US 5692160 A	Temperature, process and voltage variant slew rate based power usage simulation and method	19971125	703/23
US 5625803 A	Slew rate based power usage simulation and method	19970429	703/14
US 5537329 A	Apparatus and method for analyzing circuits	19960716	716/4
US 5446676 A	Transistor-level timing and power simulator and power analyzer	19950829	703/19
US 5283753 A	Firm function block for a programmable block architected heterogeneous integrated circuit	19940201	716/17
US 4977529 A	Training simulator for a nuclear power plant	19901211	703/18
US 4912664 A	Method and apparatus for generating a mesh for finite element analysis	19900327	716/20
US 4811237 A	Structured design method for generating a mesh power bus structure in high density layout of VLSI chips	19890307	716/9
US 4580228 A	Automated design program for LSI and VLSI circuits	19860401	716/9
US 3903399 A	System and method for converging iterations in a hybrid loadflow computer arrangement	19750902	703/3
US 3886332 A	Application of basecase results to initiate iterations and test for convergence in a hybride computer arrangement used to generate rapid electric power system loadflow solutions	19750527	703/3

US 3886330 A	Security monitoring system and method for an electric power system employing a fast on-line loadflow computer arrangement	19750527	703/3
US 3839629 A	HYBRID INTERFACING OF COMPUTATIONAL FUNCTIONS IN A HYBRID LOADFLOW COMPUTER ARRANGEMENT FOR ELECTRIC POWER SYSTEMS	19741001	703/3
US 3808409 A	LOADFLOW COMPUTER AND DC CIRCUIT MODULES EMPOLYED THEREIN FOR SIMULATING AC ELECTRIC POWER NETWORKS	19740430	703/3
US 3705409 A	TABLEAU NETWORK DESIGN SYSTEM	19721205	716/1
US 20040060024 A1	Voltage island design planning	20040325	716/7
US 20040060023 A1	Voltage island chip implementation	20040325	716/7
US 20040049754 A1	Method and apparatus for filling and connecting filler material in a layout	20040311	716/8
US 20030233219 A1	Method and apparatus emulating read only memories with combinatorial logic networks, and methods and apparatus generating read only memory emulator combinatorial logic networks	20031218	703/14
US 20030212973 A1	Methods for full-chip vectorless dynamic IR analysis in IC designs	20031113	716/6
US 20030101426 A1	System and method for providing isolated fabric interface in high-speed network switching and routing platforms	20030529	716/12
US 20030061571 A1	METHOD OF DESIGNING A VOLTAGE PARTITIONED SOLDER-BUMP PACKAGE	20030327	716/1
US 20020174409 A1	System and method for analyzing power distribution using static timing analysis	20021121	716/6
US 20020169590 A1	System and method for determining the required decoupling capacitors for a power distribution system using an improved capacitor model	20021114	703/18
US 20020112212 A1	Method for supply voltage drop analysis during placement phase of chip design	20020815	716/1
US 20020040466 A1	Automated EMC-driven layout and floor planning of electronic devices and systems	20020404	716/9
US 20010034587 A1	METHOD FOR DETERMINING THE DESIRED DECOUPLING COMPONENTS FOR POWER DISTRIBUTION SYSTEMS	20011025	703/2

Results of search set L4:

US 6675139 B1	Floor plan-based power bus analysis and design tool for integrated circuits	20040106	703/17
US 6586828 B2	Integrated circuit bus grid having wires with pre-selected variable widths	20030701	257/691
US 6583045 B1	Chip design with power rails under transistors	20030624	438/620
US 6581201 B2	Method for power routing and distribution in an integrated circuit with multiple interconnect layers	20030617	716/12
US 6577992 B1	Transistor level circuit simulator using hierarchical data	20030610	703/14
US 6574780 B2	Method and system for electronically modeling and estimating characteristics of a multi-layer integrated circuit chip carrier	20030603	716/4

US 6542834 B1	Capacitance estimation	20030401	702/65
US 6405349 B1	Electronic device parameter estimator and method therefor	20020611	716/4
US 6397170 B1	Simulation based power optimization	20020528	703/14
US 6378120 B2	Power bus and method for generating power slits therein	20020423	716/10
US 6336207 B1	Method and apparatus for designing LSI layout, cell library for designing LSI layout and semiconductor integrated circuit	20020101	716/11
US 6253354 B1	Method and apparatus for analyzing variations in source voltage of semiconductor device	20010626	716/4
US 6233721 B1	Power bus and method for generating power slits therein	20010515	716/8
US 6202196 B1	Method for optimizing routing mesh segment width	20010313	716/14
US 6195787 B1	Layout designing method for semiconductor integrated circuits	20010227	716/8
US 6090151 A	Electronic device parameter estimator and method therefor	20000718	716/5
US 6075934 A	Method for optimizing contact pin placement in an integrated circuit	20000613	716/10
US 6058257 A	Integrated circuit, design method for the same, and memory storing the program for executing the design method	20000502	716/12
US 6038383 A	Method and apparatus for determining signal line interconnect widths to ensure electromigration reliability	20000314	716/5
US 6035407 A	Accomodating components	20000307	713/300
US 5995732 A	Method and apparatus of verifying reliability of an integrated circuit against electromigration	19991130	716/5
US 5933358 A	Method and system of performing voltage drop analysis for power supply networks of VLSI circuits	19990803	703/14
US 5835378 A	Computer implemented method for leveling interconnect wiring density in a cell placement for an integrated circuit chip	19981110	700/121
US 5825673 A	Device, method, and software products for extracting circuit-simulation parameters	19981020	703/14
US 5808900 A	Memory having direct strap connection to power supply	19980915	716/10
US 5761076 A	Method for evaluating a driving characteristic of a device for a wiring, based upon lower order coefficients of series expansion form of complex admittance of the wiring	19980602	716/5
US 5737580 A	Wiring design tool improvement for avoiding electromigration by determining optimal wire widths	19980407	716/12
US 5706477 A	Circuit simulation model extracting method and device	19980106	703/14
US 5648910 A	Method of automatically optimizing power supply network for semi-custom made integrated circuit device	19970715	716/2
US 5640329 A	Method of estimating heat generated in chip	19970617	716/4
US 5625567 A	Electronic circuit design system and method with programmable addition and manipulation of logic elements surrounding terminals	19970429	716/3
US 5598348 A	Method and apparatus for analyzing the power network of a VLSI circuit	19970128	716/2

US 5581475 A	Method for interactively tailoring topography of integrated circuit layout in accordance with electromigration model-based minimum width metal and contact/via rules	19961203	716/10

Results of search set L5:

US 6683336 B1	SEMICONDUCTOR INTEGRATED CIRCUIT, SUPPLY METHOD FOR SUPPLYING MULTIPLE SUPPLY VOLTAGES IN SEMICONDUCTOR INTEGRATED CIRCUIT, AND RECORD MEDIUM FOR STORING PROGRAM OF SUPPLY METHOD FOR SUPPLYING MULTIPLE SUPPLY VOLTAGES IN SEMICONDUCTOR INTEGRATED CIRCUIT	20040127	257/207
US 6604229 B2	Method of designing wiring for power sources in a semiconductor chip, and a computer product	20030805	716/13
US 6581201 B2	Method for power routing and distribution in an integrated circuit with multiple interconnect layers	20030617	716/12
US 6405354 B1	Method and apparatus to optimize power wiring layout and generate wiring layout data for a semiconductor integrated circuit	20020611	716/8
US 6336207 B1	Method and apparatus for designing LSI layout, cell library for designing LSI layout and semiconductor integrated circuit	20020101	716/11
US 6308307 B1	Method for power routing and distribution in an integrated circuit with multiple interconnect layers	20011023	716/8
US 6308302 B1	Semiconductor wiring technique for reducing electromigration	20011023	716/5
US 6170079 B1	Power supply circuit diagram design system	20010102	716/10
US 6111310 A	Radially-increasing core power bus grid architecture	20000829	257/691
US 6097043 A	Semiconductor integrated circuit and supply method for supplying multiple supply voltages in a semiconductor integrated circuit	20000801	257/207
US 6083271 A	Method and apparatus for specifying multiple power domains in electronic circuit designs	20000704	716/1
US 6075934 A	Method for optimizing contact pin placement in an integrated circuit	20000613	716/10
US 6038383 A	Method and apparatus for determining signal line interconnect widths to ensure electromigration reliability	20000314	716/5
US 5844263 A	Semiconductor integrated device having independent circuit blocks and a power breaking means for selectively supplying power to the circuit blocks	19981201	257/208
US 5754435 A	Method and apparatus for calculating power consumption of integrated circuit	19980519	702/60
US 5737580 A	Wiring design tool improvement for avoiding electromigration by determining optimal wire widths	19980407	716/12

Results of search set L6:

US 6721933 B2	Input/output cell placement method and semiconductor device	20040413	716/10

US 6717270 B1	Integrated circuit die I/O cells	20040406	257/758
US 6674166 B2	Flip-chip integrated circuit routing to I/O devices	20040106	257/738
US 6667865 B2	Efficient design of substrate triggered ESD protection circuits	20031223	361/56
US 6661254 B1	Programmable interconnect circuit with a phase-locked loop	20031209	326/41
US 6621680 B1	5V tolerant corner clamp with keep off circuit and fully distributed slave ESD clamps formed under the bond pads	20030916	361/111
US 6584606 B1	Fast method of I/O circuit placement and electrical rule checking	20030624	716/10
US 6584596 B2	Method of designing a voltage partitioned solder-bump package	20030624	716/1
US 6523159 B2	Method for adding decoupling capacitance during integrated circuit design	20030218	716/10
US 6457157 B1	I/O device layout during integrated circuit design	20020924	716/2
US 6323559 B1	Hexagonal arrangements of bump pads in flip-chip integrated circuits	20011127	257/778
US 6243849 B1	Method and apparatus for netlist filtering and cell placement	20010605	716/8
US 6242814 B1	Universal I/O pad structure for in-line or staggered wire bonding or arrayed flip-chip assembly	20010605	257/786
US 6236230 B1	Method, architecture and circuit for product term allocation	20010522	326/39
US 6233191 B1	Field programmable memory array	20010515	365/221
US 6225143 B1	Flip-chip integrated circuit routing to I/O devices	20010501	438/106
US 6212490 B1	Hybrid circuit model simulator for accurate timing and noise analysis	20010403	703/14
US 6188242 B1	Virtual programmable device and method of programming	20010213	326/41
US 6130854 A	Programmable address decoder for field programmable memory array	20001010	365/230.06
US 6130550 A	Scaleable padframe interface circuit for FPGA yielding improved routability and faster chip layout	20001010	326/39
US 6118707 A	Method of operating a field programmable memory array with a field programmable gate array	20000912	365/189.08
US 6092226 A	Fabrication of test logic for level sensitive scan on a circuit	20000718	714/727
US 6091645 A	Programmable read ports and write ports for I/O buses in a field programmable memory array	20000718	365/189.02
US 6086627 A	Method of automated ESD protection level verification	20000711	716/5
US 6083271 A	Method and apparatus for specifying multiple power domains in electronic circuit designs	20000704	716/1
US 6075745 A	Field programmable memory array	20000613	365/230.03
US 6057169 A	Method for I/O device layout during integrated circuit design	20000502	438/14
US 6044031 A	Programmable bit line drive modes for memory arrays	20000328	365/230.03
US 6038192 A	Memory cells for field programmable memory array	20000314	365/230.03
US 6023421 A	Selective connectivity between memory sub-arrays and a hierarchical bit line structure in a memory array	20000208	365/63
US 6015732 A	Dual gate oxide process with increased reliability	20000118	438/253
US 6002268 A	FPGA with conductors segmented by active repeaters	19991214	326/41
US 5989948 A	Methods of forming pairs of transistors, and methods of forming pairs of transistors having different voltage tolerances	19991123	438/216

US 5952726 A	Flip chip bump distribution on die	19990914	257/778
US 5949719 A	Field programmable memory array	19990907	365/189.01
US 5914906 A	Field programmable memory array	19990622	365/230.03
US 5885855 A	Method for distributing connection pads on a semiconductor die	19990323	438/128
US 5847965 A	Method for automatic iterative area placement of module cells in an integrated circuit layout	19981208	716/9
US 5777354 A	Low profile variable width input/output cells	19980707	257/202
US 5760719 A	Programmable I/O cell with data conversion capability	19980602	341/100
US 5682321 A	Cell placement method for microelectronic integrated circuit combining clustering, cluster placement and de-clustering	19971028	716/8
US 5552333 A	Method for designing low profile variable width input/output cells	19960903	438/129
US 5519631 A	Method of arranging components in semiconductor device	19960521	716/10
US 5404033 A	Application specific integrated circuit and placement and routing software with non-customizable first metal layer and vias and customizable second metal grid pattern	19950404	257/202
US 5369595 A	Method of combining gate array and standard cell circuits on a common semiconductor chip	19941129	716/17
US 5119169 A	Semiconductor integrated circuit device	19920602	257/369
US 5051917 A	Method of combining gate array and standard cell circuits on a common semiconductor chip	19910924	716/17
US 4786613 A	Method of combining gate array and standard cell circuits on a common semiconductor chip	19881122	438/129
US 20040026794 A1	High speed I/O pad and pad/cell interconnection for flip chips	20040212	257/778
US 20030182640 A1	Signal integrity analysis system	20030925	716/4
US 20030178228 A1	Method for scalable architectures in stackable three-dimentsional integrated circuits and electronics	20030925	174/259
US 20030033374 A1	Method and system for implementing a communications core on a single programmable device	20030213	709/217
US 20020199155 A1	Cell modeling in the design of an integrated circuit	20021226	716/1
US 20020095647 A1	Method for adding decoupling capacitance during integrated circuit design	20020718	716/10
US 20020064064 A1	Semiconductor device, a method of manufacturing the same and storage media	20020530	365/63
US 20020056857 A1	I/O cell placement method and semiconductor device	20020516	257/203
US 20020030954 A1	Layout for efficient ESD design of substrate triggered ESD protection circuits	20020314	361/56
US 20010020746 A1	Flip-chip integrated circuit routing to I/O devices	20010913	257/778
NN9005325	LSSD Boundary-Scan Design System for Reduced Pin-Count Testing.	19900501	
NN9005205	Generalized Lssd Boundary-Scan Design System.	19900501	
NB8908417	Chip Design Exclusively by Programs	19890801	
JP 06120291 A	GATE ARRAY LSI	19940428	

EP 388189 A	Component arranger method for semiconductor device - having wiring capacitance of conductors connecting associated components in specific network lower than predetermined value	19900919
EP 1205974 A2	I/O cell placement method and semiconductor device	20020515